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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,651	04/18/2001	Robert Warren Sherburne, Jr		9125

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EXAMINER	
BUTLER, DENNIS	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,651	SHERBURNE, JR, ROBERT WARREN	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 19-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 19-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the amendment received on December 20, 2004. Claims 1-9 and 19-31 are pending. Claims 10-18 have been canceled. Claims 21-31 have been added.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-6, 9 and 27-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiyama et al., U. S. Patent 5,790,877.

Per claims 1 and 27-28:

A) Nishiyama et al teach the following claimed items:

1. an integrated circuit with processor 100 of figure 1;

2. a plurality of processor units each having a clock input that controls the performance of the unit with elements 103, 104 and 105 figure 1, at column 2, lines 37-41 and at column 3, lines 43-49;

3. a controller having a plurality of clock outputs each coupled to respective clock inputs of the processor units with CLK CONT 101 of figure 1 and at column 3, lines 43-60;

4. the controller varying the clock frequency of each processor unit at column 2, lines 51-65, at column 3, lines 50-67 and at column 6, lines 8-17.

Per claims 3-6, 9, 29 and 30:

Nishiyama describes at least one of the processor units comprises a RISC processor at column 3, lines 35-42. Nishiyama describes dynamically managing each processor unit on a per task basis at column 2, lines 37-65, at column 3, lines 50-67 and at column 6, lines 9-18. Nishiyama describes each unit clocked at the lowest rate possible to reduce peak power dissipation or average dissipation at column 2, lines 52-60 and at column 6, lines 9-18. Nishiyama describes the controller generating a plurality of clock signals with figure 2 and independently controlling the rate to each processor unit at column 3, lines 64-67 and at column 4, lines 21-34.

5. Claims 2, 7-8 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama et al., U. S. Patent 5,790,877 in view of Georgiou et al., U. S. Patent 6,047,248.

Per claims 2, 7 and 8:

Nishiyama et al teach the items of claims 1 and 6 as described above. The claims seem to differ from Nishiyama et al in that Nishiyama et al fails to explicitly teach at least one of the processor units comprising a DSP or the plurality of clocks being gated versions of a master clock as claimed. Georgiou teaches that it is known to provide a controller that outputs a plurality of clocks to one or more DSP processor units at column 3, lines 61-65. In addition, Georgiou teaches that it is known to provide gated versions of a master clock with figure 4 and at column 8, lines 37-67. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a controller that outputs a plurality of clocks to one or more DSP processor units or to provide gated versions of a master clock, as taught by Georgiou, in order to apply Nishiyama's power saving system to a processor core having at least one DSP processing unit or to provide the details of implementing Nishiyama's clock generator of figure 2. One of ordinary skill in the art would have been motivated to combine Nishiyama and Georgiou because of Georgiou's suggestion that a clock control system having a plurality of clock outputs coupled to a plurality of functional units can be applied to DSP functional units at column 3, lines 48-65 and because of Nishiyama's suggestion that the clock generator provide a multi-frequency dividable clock for each hardware resource at column 4, lines 31-35. It would have been obvious for one of ordinary skill in the art to combine Nishiyama and Georgiou because they are both directed to the problem of reducing the

power consumption of a processor by individually controlling the clock frequency to each processor/functional unit.

Per claims 19-20:

Georgiou describes a buffer coupled between two processing units with Completion Unit 122 of figure 1 and at column 6, lines 5-7 and 25-29. Georgiou does not explicitly describe using a FIFO buffer. However, FIFO buffers are well known in the art and it would have been obvious to use a FIFO buffer in order to process instructions in a first in first out manner.

6. Claims 21-23 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama et al., U. S. Patent 5,790,877 in view of Asghar et al., U. S. Patent 5,790,817.

Per claims 21-23 and 26:

Nishiyama et al teach the items of claim 1 as described above. The claims seem to differ from Nishiyama et al in that Nishiyama et al fails to explicitly teach the integrated circuit including first and second wireless transceivers on the single substrate and including a buffer between first and second processor units as claimed. Asghar teaches that it is known to including first and second wireless transceivers on the single substrate with Transmit DSPs 212a and Receive DSPs 212b of figure 2, at column 5, lines 2-5, at column 7, lines 22-37 and at column 7, line 45 – column 8, line 16. Asghar describes including a buffer between first and second processor units with System Memory 202 of figure 2 and at column 5, lines 6-21. It would have been obvious to one having ordinary skill in the art at

the time the invention was made to include first and second wireless transceivers on the single substrate, as taught by Asghar, in order to apply Nishiyama's power saving system to a processor core having wireless communication capabilities. One of ordinary skill in the art would have been motivated to combine Nishiyama and Asghar because of Asghar's suggestion of implementing wireless receivers and transmitters using a plurality of DSP units in order to reduce power consumption at column 7, lines 45-67 and because of Nishiyama's suggestion that the clock generator provide a multi-frequency dividable clock for each hardware resource at column 4, lines 31-35. It would have been obvious for one of ordinary skill in the art to combine Nishiyama and Asghar because they are both directed to the problem of reducing the power consumption of a processor by controlling the clock frequency to the processor units.

Per claims 24 and 25:

A) Nishiyama et al teach the following claimed items:

1. an integrated circuit with processor 100 of figure 1;

2. a plurality of processor units each having a clock input that controls the performance of the unit with elements 103, 104 and 105 figure 1, at column 2, lines 37-41 and at column 3, lines 43-49;

3. a controller having a plurality of clock outputs each coupled to respective clock inputs of the processor units with CLK CONT 101 of figure 1 and at column 3, lines 43-60;

4. the controller varying the clock frequency of each processor unit at column 2, lines 51-65, at column 3, lines 50-67 and at column 6, lines 8-17.

B) The claims seem to differ from Nishiyama et al in that Nishiyama et al fails to explicitly teach the integrated circuit including first and second wireless transceivers on the single substrate and including a display as claimed.

C) Asghar teaches that it is known to including first and second wireless transceivers on the single substrate with Transmit DSPs 212a and Receive DSPs 212b of figure 2, at column 5, lines 2-5, at column 7, lines 22-37 and at column 7, line 45 – column 8, line 16. Asghar describes that the invention is directed to a digital cellular device for wireless communications with figure 1 and at column 4, lines 45-59. Digital cellular devices inherently include a display for displaying phone numbers and other text and graphic information. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include first and second wireless transceivers on the single substrate, as taught by Asghar, in order to apply Nishiyama's power saving system to a processor core having wireless communication capabilities. One of ordinary skill in the art would have been motivated to combine Nishiyama and Asghar because of Asghar's suggestion of implementing wireless receivers and transmitters using a plurality of DSP units in order to reduce power consumption at column 7, lines 45-67 and because of Nishiyama's suggestion that the clock generator provide a multi-frequency dividable clock for each hardware resource at column 4, lines 31-35. It would have been obvious for one of ordinary skill in the art to combine

Nishiyama and Asghar because they are both directed to the problem of reducing the power consumption of a processor by controlling the clock frequency to the processor units.

7. Claims 1, 27-28 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Nicol et al., U. S. Patent 6,141,762.

Per claim 1

A) Nicol et al teach the following claimed items:

1. an integrated circuit with the Chip of figure 4;

2. a plurality of processor units each having a clock input that controls the performance of the unit with the PEs of figure 4 and at column 5, line 53 – column 6, line 2;

3. a controller having a plurality of clock outputs each coupled to respective clock inputs of the processor units with the three PLLs and the Controller of figure 4 and at column 6, lines 2-13;

4. the controller varying the clock frequency of each processor unit with figure 3 and at column 5, line 66 – column 6, line 9.

Per claim 27:

A) Nicol et al teach the following claimed items:

1. generating a plurality of clock signals on an integrated circuit (Chip) that are variable under the control of a controller on the integrated circuit with the clock signals output by the PLLs of figure 4 and at column 5, line 53 – column 6, line 9;

2. providing each of the clock signals to a corresponding one of a plurality of processor units (PEs) on the integrated circuit with the clock signals input to each of the PEs of figure 4 and at column 5, line 66 – column 6, line 2.

Per claims 28 and 30:

Nicol describes varying at least one of the clock signals using the controller and independently rate controlling each of the clock signals at column 5, line 66 – column 6, line 9.

8. Claims 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicol et al., U. S. Patent 6,141,762 in view of Asghar et al., U. S. Patent 5,790,817.

Per claims 29 and 31:

Nicol et al teach the items of claim 27 as described above. The claims seem to differ from Nicol et al in that Nicol et al fails to explicitly teach dynamically managing the clock signal for a processor unit on a per-task basis and providing a clock signal controlled by the controller to a wireless transceiver on the integrated circuit as claimed. However, Nicol describes independently programming the lowest operating frequency for each PE at column 5, line 66 – column 6, line 2. Asghar describes that it is known to dynamically manage the clock signal for a processor unit on a per-task basis with Microcontroller 222 of figure 2 and at column 5, line 56 – column 6, line 17. In addition, Asghar teaches that it is known to include a wireless transceiver on the integrated circuit that has a clock controlled by the controller (Microcontroller 222) with Transmit DSPs 212a and Receive DSPs 212b of figure 2, at column 5, lines 2-5, at column 7,

lines 22-37 and at column 7, line 45 – column 8, line 16. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include first and second wireless transceivers on the single substrate, as taught by Asghar, in order to apply Nishiyama's power saving system to a processor core having wireless communication capabilities. One of ordinary skill in the art would have been motivated to combine Nicol and Asghar because of Asghar's suggestion of implementing wireless receivers and transmitters using a plurality of DSP units in order to reduce power consumption at column 7, lines 45-67 and because of Nicol's suggestion of independently programming the lowest operating frequency for each PE in order to reduce power consumption at column 5, line 66 – column 6, line 2. It would have been obvious for one of ordinary skill in the art to combine Nicol and Asghar because they are both directed to the problem of reducing the power consumption of a multiprocessor system by controlling the clock frequency to the processor units.

9. In the amendment received on June 8, 2004, applicant amended the claims from "processing units" to "processor units" and argued that processor units are whole processors. In response to these amendments and arguments, the examiner withdrew the rejection of the claims based on Nishiyama et al. However, the examiner no longer agrees that the "processor units" recitation limits these units to whole processors as argued. The specification is directed to processing units as first recited in the claims. Figures 2-5 show that the units are not limited to whole processors. In addition, the specification describes that processing units include functional units and execution units

that are part of a processor core. The specification describes several embodiments that include units that are not whole processors and includes disclaimer statements that the invention is not limited to the particular embodiments described and that numerous modifications, rearrangements and substitutions are capable. Furthermore, the claims do not recite "whole processors" as argued. Therefore, the claims are not limited to whole processor and Nishiyama et al has been reapplied to the claimed invention.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 571-272-3663.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dennis M. Butler
Primary Examiner
Art Unit 2115